

| Very Large Scale Integration (VLSI) |                                                                                                                                                              |                                                          |
|-------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------|
| Introduction to VLSI                | What is VLSI? History and significance<br>VLSI applications in industry<br>VLSI design flow overview<br>Tools used in VLSI design (EDA tools)                | 04th October (07:10-08:10)<br>06th October (07:10-08:10) |
| Digital Electronics Fundamentals    | Number systems and Boolean algebra<br>Logic gates and truth tables<br>Combinational vs. Sequential logic<br>Basic circuits: adders, multiplexers, flip-flops | 07th October (07:10-08:10)<br>08th October (07:10-08:10) |
| CMOS Technology Basics              | Introduction to MOSFETs (NMOS & PMOS)<br>CMOS inverter characteristics<br>CMOS logic gate design (NAND, NOR, etc.)<br>Power dissipation and delay            | 09th October (07:10-08:10)<br>11th October (06:00-07:00) |
| Verilog/VHDL Basics                 | HDL overview and applications<br>Verilog/VHDL syntax and data types<br>Modules, ports, and assignments<br>Writing simple combinational logic                 | 12th October (06:00-07:00)<br>14th October (06:00-07:00) |
| Sequential Logic in Verilog/VHDL    | Flip-flops and latches in HDL<br>Finite State Machines (FSMs)<br>Writing and simulating counters, registers<br>Testbenches for sequential designs            | 15th October (06:00-07:00)<br>19th October (06:00-07:00) |
| RTL Design and Verification         | Register Transfer Level (RTL) modeling<br>Behavioral vs Structural design<br>Simulation using tools (e.g., ModelSim)<br>Debugging and waveform analysis      | 22th October (06:00-07:00)<br>24th October (06:00-07:00) |
| Synthesis Concepts                  | From RTL to gates: Logic synthesis<br>Setup and hold times, critical path<br>Timing analysis basics<br>Area vs speed vs power trade-offs                     | 27th October (06:00-07:00)                               |
| FPGA Architecture and Design        | Introduction to FPGA structure<br>Differences between ASIC and FPGA<br>Toolchain overview (Vivado, Quartus)<br>Simple design implementation on FPGA          | 30th October (06:00-07:00)                               |
| ASIC Flow Introduction              | ASIC design flow overview<br>Floorplanning, placement, routing (basics)<br>Standard cell libraries<br>Fabrication process overview                           | 01st November (06:00-07:00)                              |

|                          |                                                                                                                                                             |                             |
|--------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|
| Major Project and Review | Major project (e.g., 4-bit ALU, traffic controller)<br>Design, simulate, and synthesize<br>Project report preparation<br>Feedback and internship completion | 02nd November (06:00-07:00) |
|--------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|